Thermoelectric Cooler (TEC) Controller

Preliminary Technical Data

ADN8831

FEATURES

On-Chip temperature measurement amplifiers
TEC current voltage monitoring
Programmable maximum TEC voltage
Programmable maximum TEC current
Separate heating and cooling current limits
High efficiency: >90%
Temperature lock indication
Programmable switching frequency up to 1MHz
Oscillator synchronization with an external signal
Clock phase adjustment for multiple operation
Compact 5mm x 5mm LFCSP

APPLICATIONS

Thermoeletric Cooler(TEC) control
Optical Transceiver Modules
Optical Fibre Amplifiers
Optical Netwroking systems

GENERAL DESCRIPTION

The ADN8831 is a monolithic controller that drives a Thermoelectric Cooler (TEC) to stabilize the temperature of a laser diode or a passive component used in communications equipment.

This device relies on a Negative Temperature Coefficient (NTC) thermistor or a positive temperature coefficient RTD device to sense the temperature of the object attached to the TEC. The target temperature is set with an analog input voltage either from a DAC or with an external resistor divider.

The loop is stabilized by a PID compensation amplifier with high stability and low noise. The compensation network can be adjusted by the user to optimize temperature settling time.

The ADN8831 measures and limits a TEC current for both heating and cooling independently. A 2.5V voltage references is provided for the thermistor temperature sensing bridge.

FUNCTIONAL BLOCK DIAGRAM

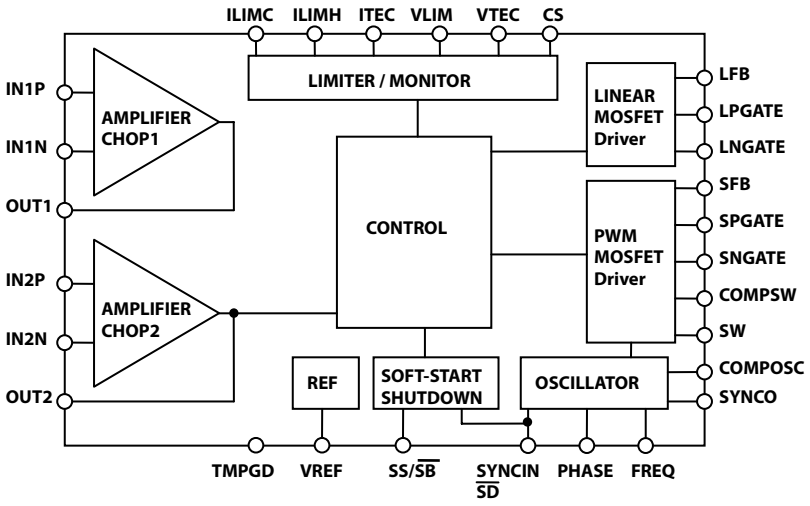

Figure 1.

Rev. PrD

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

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REVISION HISTORY

6/05 – Rev. PrC to Rev. PrD

Changes to SPECIFICATION

Added FUNCTIONAL DESCRIPTION

SPECIFICATIONS

Table I. ADN8831—Electrical Characteristics (V_{DD} = 3.0 V to 5.0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PWM OUTPUT DRIVERS						
Output Transition Time	t_R, t_F	C_L = 3,300 pF		20		ns
Nonoverlapping Clock Delay			50	65		ns
Output Resistance	$R_{O(N1,P1)}$	I_L = 10 mA, V_{DD} = 3.3V		6		Ω
Output Voltage Swing	SFB	V_{LIM} = VREF	0		V_{DD}	V
LINEAR OUTPUT AMPLIFIER						
Output Resistance	$R_{O, LNGATE}$ $R_{O, LPGATE}$	I_{OUT} = 2 mA, V_{DD}=3.3V I_{OUT} = 2 mA, V_{DD}=3.3V		175 100		Ω Ω
Output Voltage Swing	LFB		0		V_{DD}	V
POWER SUPPLY						
Power Supply Voltage	V_{DD}		3.0		5.5	V
Supply Current	I_{SY}	PWM not switching -40°C ≤ T_A ≤ +85°C		8	12 15	mA mA
Shutdown Current	I_{SD}	SYNCIN/$\overline{SD}$ = 0 V		5		µA
Soft-Start Charging Current	I_{SS}			2		µA
Undervoltage Lockout	UVLO	Low to high threshold		2.1	2.5	V
Standby Current	I_{SB}	SINCIN/$\overline{SD}$ = V_{DD}, SS/SB = 0 V		2		mA
Standby Threshold	V_{SB}	SYNCIN/$\overline{SD}$ = V_{DD}		200	300	mV
ERROR / Compensation AMPLIFIERS						
Input Offset Voltage	V_{OS1} V_{OS2}	V_{CM1} = 1.5 V, V_{IN1P} – V_{IN1M} V_{CM2} = 1.5 V, V_{IN2P} – V_{IN2M}		10 10	100 100	µV µV
Input Voltage Range	$V_{CM1,2}$		0		V_{DD}	V
Common-Mode Rejection Ratio	$CMRR_{1,2}$			120		dB
Output Voltage Range	$V_{OUT1,2}$		0		V_{DD}	V
Power Supply Rejection Ratio	$PSRR_{1,2}$	3.0 V ≤ V_{DD} ≤ 5.0 V		120		dB
Output Current	$I_{OUT1,2}$		-5		+5	mA
Gain Bandwidth Product	$GBW_{1,2}$	V_{OUT} = 0.5V to (V_{DD}-1V)		2		MHz
OSCILLATOR						
Sync Range	f_{CLK}	SYNCIN/$\overline{SD}$ connected to external clock	200		1,000	KHz
Oscillator Frequency	f_{CLK}	COMPOSC = V_{DD}, RFREQ = 180kΩ, SYNCIN/$\overline{SD}$ = V_{DD}	800	1,000	1,250	kHz
Free-Run Oscillation Frequency	f_{CLK}	COMPOSC = V_{DD}, SYNCIN/$\overline{SD}$ = V_{DD}	100		1000	KHz
Phase Adjustment Range	Φ_{CLK}	0.1 V ≤ V_{PHASE} ≤ 2.4 V	25		335	°
Phase Adjustment Default	Φ_{CLK}	PHASE = open		180		°
REFERENCE VOLTAGE						
Reference voltage	V_{REF}	I_{REF} < 2mA	2.37	2.47	2.57	V
LOGIC OUTPUTS						
Logic Low Output Voltage	V_{OL}	TEMPGD, SYNCOUT, I_O=0 A			0.2	V
Logic High Output Voltage	V_{OH}	TEMPGD, SYNCOUT, I_O=0 A	V_{DD} - 0.2V			V
Output Impedance		V_{DD}=5.0 V		100		Ω
		V_{DD}=3.3 V		140		Ω
Output Current	I_O				10	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TEC CURRENT MEASUREMENT						
ITEC Gain	$A_{V,ITEC}$	$V_{ITEC}/(V_{LFB}-V_{CS})$		25		V/V
ITEC Output Range	V_{ITEC}		0		V_{DD}	V
ITEC Input Range	$V_{CS, VLFB}$		0		V_{DD}	V
ITEC Bias Voltage	$V_{ITEC, B}$	$V_{LFB} = V_{CS} = 0$	1.2	1.25	1.3	V
ITEC Output Current	$I_{OUT,TEC}$			1		mA
TEC VOLTAGE MEASUREMENT						
VTEC Gain	$A_{V,VTEC}$	$V_{VTEC}/(V_{LFB}-V_{SFB})$	0.23	0.25	0.27	V/V
VTEC Output Range	V_{VTEC}		0		2.5	V
VTEC Bias Voltage	$V_{VTEC,B}$	$V_{LFB} = V_{SFB} = 2.5V$	1.2	1.25	1.3	V
VTEC Output Load Resistance	R_{VTEC}	I_C= 300µA		300		Ω
VOLTAGE LIMIT						
VLIM Gain	$A_{V,LIM}$	V_{SFB}/V_{VLIM}		5		V/V
VLIM Input Range	V_{VLIM}		0		V_{DD}	V
VLIM Input Current, cooling	$I_{VLIM,COOL}$	$V_{OUT2} < V_{DD}/2$			100	nA
VLIM Input Current, heating	$I_{VLIM,HEAT}$	$V_{OUT2} > V_{DD}/2$		I_{FREQ}		mA
VLIM Input Current Accuracy, heating	$I_{VLIM,HEAT}$	I_{VLIM}/I_{FREQ}	0.9	1.0	1.1	A/A
CURRENT LIMIT						
ILIMC Input Voltage Range	V_{ILIMC}		1.25		V_{DD}-1	V
ILIMH Input Voltage Range	V_{ILIMH}		0.1		1.25	V
ILIMC Limit Threshold	$V_{TH,ILIMC}$	V_{ITEC} = 2.0V	1.98	2.0	2.02	V
ILIMH Limit Threshold	$V_{TH,ILIMH}$	V_{ITEC} = 0.5V	0.475	0.5	0.525	V
TEMPERATURE GOOD						
High Threshold	$V_{OUT1,TH1}$	IN2M tied to OUT2, V_{IN2P} = 1.5V		1.525	1.530	V
Low Threshold	$V_{OUT1,TH2}$	IN2M tied to OUT2, V_{IN2P} = 1.5V	1.470	1.475		V

ABSOLUTE MAXIMUM RATINGS

Table II. Absolute Maximum Ratings (at 25°C, unless otherwise noted)

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to Vs + 0.3V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Operating Junction Temperature	125°C
Lead Temperature Range (Soldering, 60 Sec)	300°C

Table III. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
32-lead LFCSP (ACP)	35	10	°C/W

[1] θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these products feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

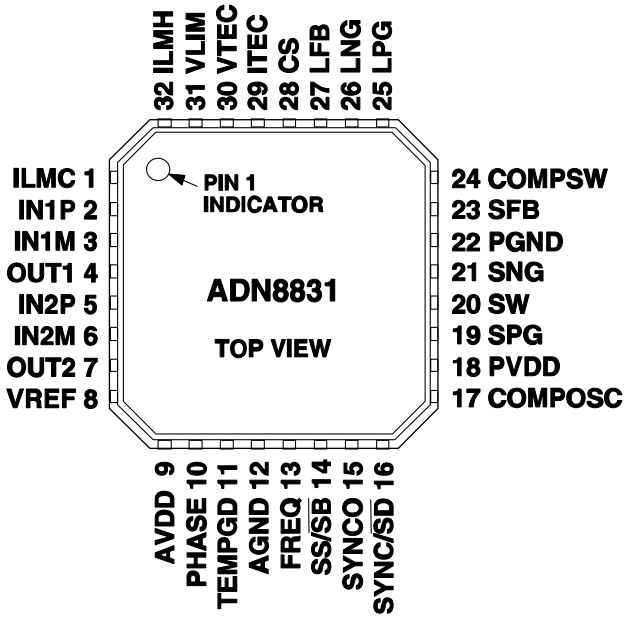

Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Mneumonic	Type	Description
1	ILIMC	Analog Input	Sets TEC cooling current limit.
2	IN1P	Analog Input	Non-inverting input to error amplifier.
3	IN1M	Analog Input	Inverting input to error amplifier.
4	OUT1	Analog Output	Output of error amplifer.
5	IN2P	Analog Input	Non-inverting input to compensation amplifier.
6	IN2M	Analog Input	Inverting input to compensation amplifier.
7	OUT2	Analog Output	Output of compensation amplifier.
8	VREF	Analog Output	2.5V Voltage Reference output.
9	AVDD	Power	Power for non-driver sections. 3.0 V min; 5.5V max.
10	PHASE	Analog Input	Sets SYNCOUT clock phase relative to SYNCIN clock.
11	TMPGD	Digital Output	Logic output. Active High. Indicates when OUT1 voltage is within ±30mV of TEMPSET voltage.
12	AGND	Ground	Analog ground. Connect to low noise ground.
13	FREQ	Analog Input	Sets switching frequency with an external resistor.
14	SS/$\overline{SB}$	Analog Input	Sets soft-start time for output voltage. Pull low to put ADN8831 into standby mode (VTEC = 0V).
15	SYNCO	Digital Output	Phase adjustment clock output. Phase set from PHASE pin. Used to drive SYNCIN of other ADN8831 devices.
16	SYNCI/$\overline{SD}$	Digital Input	Optional clock input. If not connected, clock frequency is set by FREQ pin. Pull low to put ADN8831 into shutdown mode. Pull high to negate shutdown mode.
17	COMPOSC	Analog Output	Comensation for oscillator. connect to PVDD when free-run mode, connect to R-C network when external clock mode.
18	PVDD	Power	Power for output driver sections. 3.0V min; 5.5V max.
19	SPGATE	Analog Output	PWM output drives external PMOS gate.
20	SW	Analog Input	Connects to PWM FET drains.
21	SNGATE	Analog Output	PWM output drives external NMOS gate.
22	PGND	Ground	Power ground. External NMOS devices connect to PGND. Connect to digital ground.
23	SFB	Analog Input	PWM feedback. Connect to TEC- pin of TEC.

24	COMPSW	Analog Input	Comensation for switching amplifier.
25	LPGATE	Analog Ouput	Linear output drives external PMOS gate.
26	LNGATE	Analog Output	Linear output drives external NMOS gate.
27	LFB	Analog Input	Linear feedback. Connect to TEC+ pin of TEC.
28	CS	Analog Input	Connect to output current sense resistor.
29	ITEC	Analog Ouput	Indicates TEC current.
30	VTEC	Analog Ouput	Indicates TEC voltage.
31	VLIM	Analog Input	Sets maximum TEC voltage.
32	ILIMH	Analog Input	Sets TEC heating current limit.

DETAILED BLOCK DIAGRAM

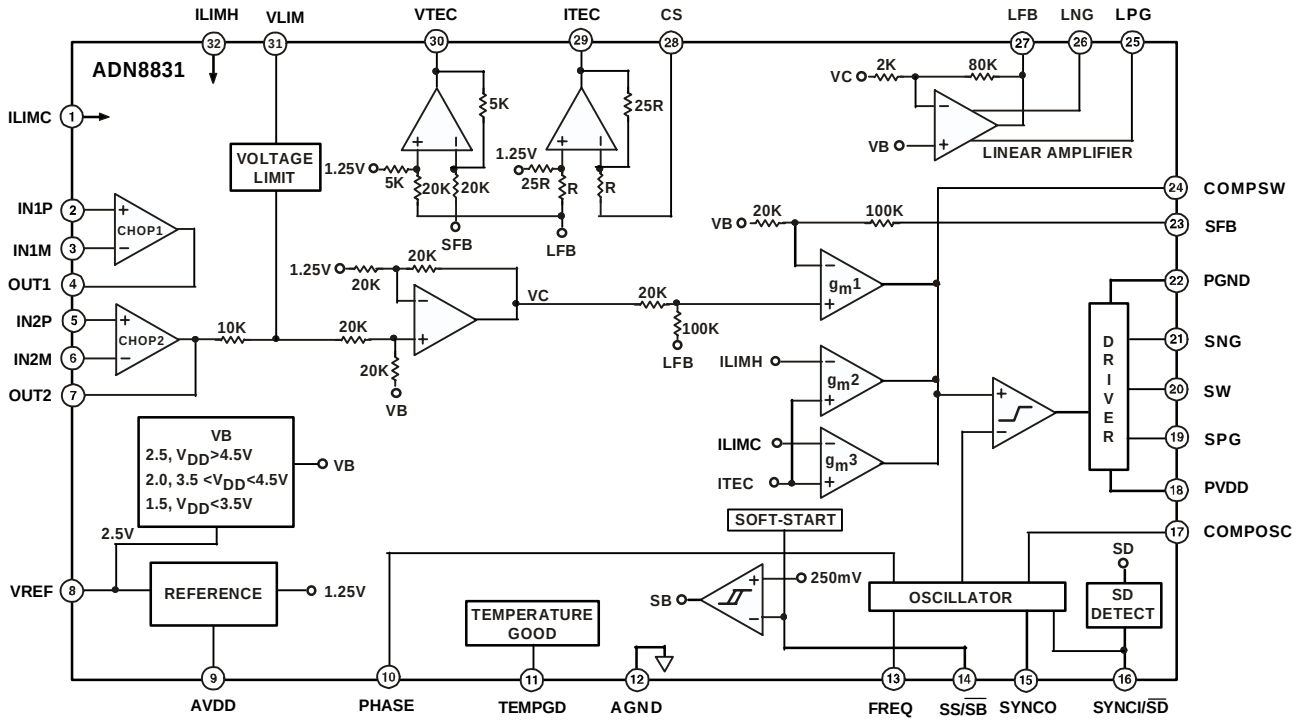

Figure 3. Detailed Block Diagram

FUNCTIONAL DESCRIPTION

INTRODUCTION

The ADN8831 is a controller for a thermoelectric cooler(TEC). A voltage applied to the input of the ADN8831 corresponds to a target temperature set point. The appropriate current is then applied to the TEC to pump heat either to or away from the object whose temperature is being regulated. The temperature of the object is measured by a thermistor and is fed back to the ADN8831 to correct the loop and settle the TEC to the appropriate final temperature. For best stability, the thermistor should be mounted in close proximity to the object. In most laser diode modules, the TEC and thermistor are already mounted in the unit and are used to regulate the temperature of the laser diode.

The ADN8831 integrates self correcting auto-zero amplifiers (chop1 and chop2). The chop 1 amplifier can be used as temperature measurement amplifier to create a voltage that is proportional to object temperature. The output of the temperature measurement amplifier(Chop1) is then fed into the compensation amplifier (Chop 2). In a compensation stage, the temperature measurement voltage is compared against the temperature set input voltage, creating an error voltage that is proportional to their difference. Also an external network consisting of a few resistors and capacitors is connected around the compensation amplifier. This network can be adjusted by the user to optimize the step response of the TEC's temperature either in terms of settling time or maximum current change. Details of how to adjust the compensation network are given in the Compensation Loop section.

The TEC is driven differentially using an H-bridge configuration. The ADN8831 drives external transistors that are used to provide the current to the TEC. To further improve the power efficiency of the system, one side of the H-bridge uses a switched output. Only one inductor and one capacitor are required to filter out the switching frequency. The other side of the H-bridge uses linear output which does not require any additional circuitry. This proprietary configuration allows the ADN8831 to provide efficiency of >90%. For most applications, a 4.7uH inductor, a 22uF capacitor and a switching frequency of 1MHz maintains less than 0.5% worst-case output voltage ripple across the TEC.

The maximum voltage across the TEC and current flowing through the TEC can be set using the VLIM and ILIM pins. Additional details are provided in the Setting Voltage and Current Limits section.

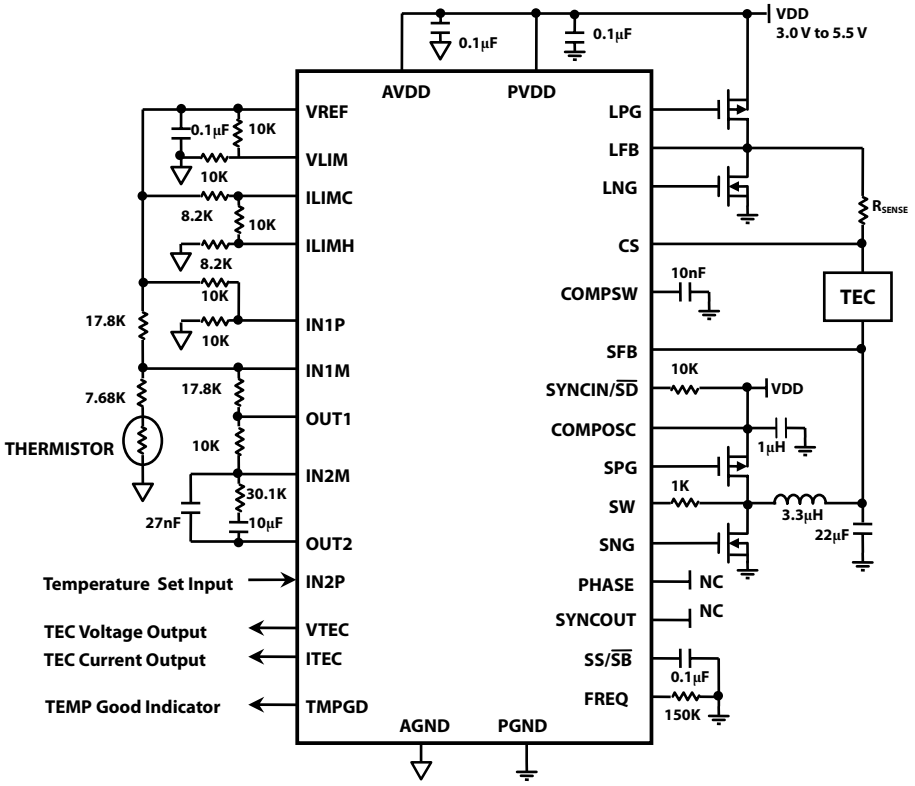

Figure 4. Typical Application Circuit I

OSCILLATOR CLOCK FREQUENCY

The ADN8831 has an internal oscillator to generate the switching frequency for the output stage. This oscillator can be either set in free-run mode or synchronized to an external clock signal.

Free-Run Operation

The switching frequency is then set by a single resistor connected from FREQ (Pin13) to ground. Table IV shows R_{FREQ} for some common switching frequencies. For free-run operation, SYNCI (Pin 16) and COMPOSC (Pin 17) should be connected to PVDD.

Table IV.

f_{SWITCH}	R_{FREQ}
100 kHz	1.28 MΩ
250 kHz	484 kΩ
500 kHz	249 kΩ
750 kHz	168 kΩ
1 MHz	118 kΩ

Higher switching frequencies reduce the voltage ripple across the TEC. However, high switch frequencies will create more power dissipation in the external transistors. This is due to the more frequent charging and discharging of the transistor's gate capacitances.

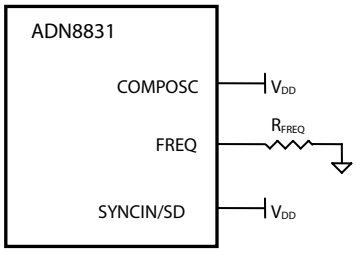

Figure 5. Free-Run Mode

External Clock Operation

The switching frequency of the ADN8831 can be synchronized with an external clock by connecting the clock signal to SYNCIN(Pin 16). The COMPOSC (Pin 17) should also be connected to an R-C network. This network is simply used to compensate a PLL to lock on to the external clock. To ensure the quickest synchronization lock-in time, the switch frequency should be set at 100kHz.

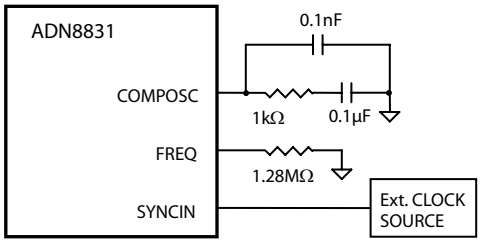

Figure 6. Synchronize to an External Clock

Connecting Multiple ADN8831 Devices

Connecting the SYNCO to the SYNCI pin of another ADN8831 allows multiple ADN8831s to be driven using a single clock. Multiple ADN8831 devices can be either driven from a single master ADN8831 device by connecting its SYNCOUT pin to each slave's SYNCIN pin or daisy-chained by connecting each device's SYNCOUT to the next device's SYNCIN pin. When multiple ADN8831 devices are clocked at same frequency, adjusting its phase should be taken into account to reduce power supply ripple.

OSCILLATOR CLOCK PHASE

The oscillator clock phase can be adjusted using a simple resistor divider at the PHASE pin. Phase adjustment allows two or more ADN8831 devices to operate from the same clock frequency and not have all outputs switch simultaneously, which could create excessive power supply ripple.

V_{PHASE} should remain between 100mV and 2.4V to ensure the oscillator operates correctly. If the PHASE pin is left open, clock phase is set at 180° as default.

TEMPERATURE LOCK INDICATOR

The TEMPGD pin (Pin11) outputs a logic HIGH when the OUT1 voltage reaches to the IN2P voltage. The TEMPGD has a detection range of ± 25 mV and a 10mV typical hysteresis. This allows direct interfacing to the micro-controllers or supervisory circuitry.

SOFT START ON POWER-UP

The ADN8831 can be programmed to ramp up for a specified time after the power supply is applied or after shutdown is de-asserted. This feature, know as soft start is useful for gradually increasing the duty cycle of the PWM amplifier. The soft start time is set with as single capacitor connected from SS (Pin 14) to ground , which capacitor value can be calculated by

$$\tau_{SS} = 150 \times C_{SS}$$

Where C_{SS} is the value of the capacitor in microfarads, and τ_{SS} is the soft start time in milliseconds. To set a soft start time of

15ms, CSS should equal 0.1uF.

SHUTDOWN MODE

The ADN8831 has a shutdown mode that sets the ADN8831 into an ultra low current state. The current draw for the ADN8831 in shutdown is typically 5µA. The shutdown input $\overline{SD}$ pin (Pin 16) is active low. To shut the device, the $\overline{SD}$ should be driven to logic low. Once a logic HIGH is applied, the ADN8331 will reactivate after the delay set by the Soft-Start circuitry. Refer to the Soft-Start section for more details on this feature.

STANDBY MODE

The ADN8831 has a standby mode that deactivates a MOSFET Driver stage. The current draw for the ADN8831 in the standby is less than 1mA. The standby input $\overline{SB}$ pin (Pin 14) is active low. Once a logic high is applied, the ADN8331 will reactivate after the delay.

TEC VOLTAGE/CURRENT MONITOR

TEC voltage and current can be monitored at the VTEC and ITEC pin respectively.

Voltage Monitor

The VTEC is an analog voltage output pin which voltage is proportional to the actual voltage across the TEC. A center voltage of the 1.25 V corresponds to 0 V across TEC. The output voltage can be calculated as follows:

$$V_{VTEC} = 1.25 + 0.25 \times (V_{LFB} - V_{SFB})$$

Current Monitor

The ITEC is an analog voltage output pin which voltage is proportional to the actual current through the TEC. A center voltage of the 1.25 V corresponds to 0 A through the TEC. The output voltage can be calculated as follows:

$$V_{ITEC} = 1.25 + 25 \times (V_{LFB} - V_{CS})$$

The TEC current is obtained from this voltage by the following equation:

$$I_{TEC} = \frac{V_{ITEC} - 1.25}{25 \times R_{SENSE}}$$

MAXIMUM TEC VOLTAGE LIMIT

The maximum TEC voltage can be set by applying a voltage at the VLIM pin to protect the TEC. This voltage can be set with either a resistor divider or from a DAC. The voltage limiter operates in bidirectional TEC voltage, cooling and heating voltage.

Using a DAC

Both the cooling and heating voltage limits will be set at same level when the VLIM pin is driven directly by a voltage source. The maximum TEC voltage is given as

$$V_{TEC(MAX)} = 5 \times V_{VLIM}$$

Where $V_{TEC(MAX)}$ is the maximum TEC voltage, V_{VLIM} is the voltage applied at VLIM pin.

Using a resistor divider

Separate voltage limits can be set with using a resistor divider. The internal current sink circuitry connected to the VLIM pin draws a current when the ADN8831 drives the TEC in heating direction which then lowers the voltage at the VLIM. The current sink is not active when the TEC is driven in a cooling direction which means that the TEC heating voltage limit is always lower than the cooling voltage limit.

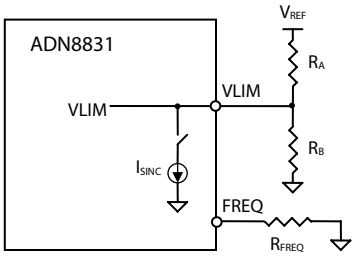

Figure 7. Using a resistor divider

The sink current is set by the resistor connected from FREQ pin to ground. The sink current is calculated as follows:

$$I_{SINK} = \frac{1.25}{R_{FREQ}}$$

Where I_{SINC} is the sink current at the VLIM pin, R_{FREQ} is the resistor connected at FREQ. Then, the cooling and heating limits are calculated as follows:

$$V_{VLIM,COOL} = \frac{V_{REF} \times R_B}{R_A + R_B}$$

$$V_{VLIM,HEAT} = V_{VLIM,COOL} - I_{SINK} \times R_A \| R_B$$

MAXIMUM TEC CURRENT LIMIT

Separate maximum TEC current limits in cooling and heating direction can be set by applying a voltage at the ILIMC and ILIMH pin to protect the TEC. Maximum TEC current are given as:

$$V_{ILIMC} = 1.25 + 25(I_{TEC,MAX,COOL} \times R_{SENSE})$$

$$V_{ILIMH} = 1.25 - 25(I_{TEC,MAX,HEAT} \times R_{SENSE})$$

OUTLINE DIMENSIONS

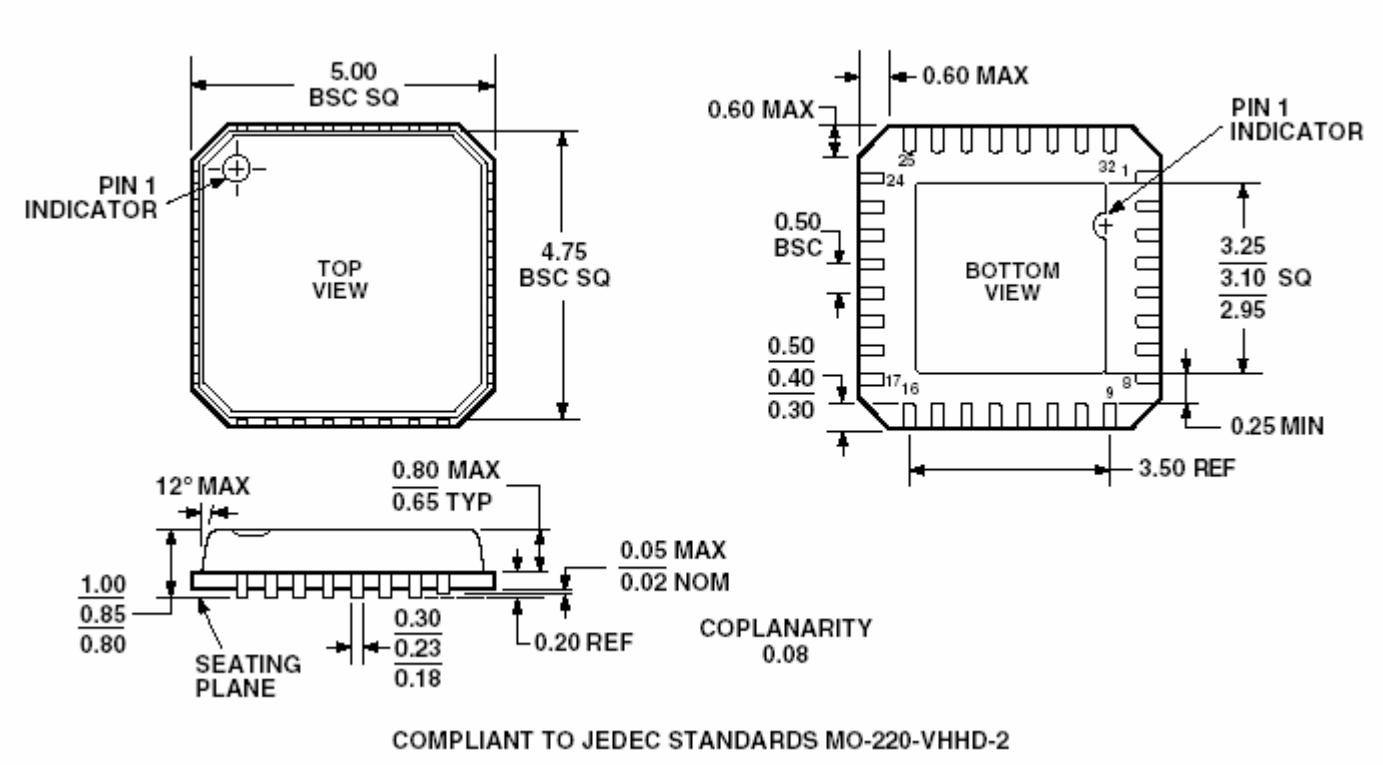

Figure 8. 32-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-32)
Dimensions Shown in Millimeters

ESD CAUTION

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ORDERING GUIDE

Table V.

Model	*Temperature Range*	*Package Description*	*Package Option*
ADN8831ACP	*-40℃ to +85℃*	*32-Lead Lead Frame Chip Scale Package*	*CP-32*
ADN8831-EVAL	*-40℃ to +85℃*	*Evaluation Board*	

PR04663-0-6/05(PrD)